This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPWRD.2015.2465152, IEEE Transactions on Power Delivery

Current Source Modular Multilevel Converter: Detailed Analysis and STATCOM Application

Mukesh M. Bhesaniya, *Student Member, IEEE,* and Anshuman Shukla, *Member, IEEE*

***Abstract*—Multilevel current source converters are a smart choice for the high power applications with low voltage and high current requirements. This paper presents the detailed analysis of a current source modular multilevel converter (CSMMC) and its application as a STATCOM. Various properties of CSMMC are correlated with the voltage source modular multilevel converter (VSMMC). Submodule inductance selection method and a sorting based algorithm for inductor current balancing are proposed for CSMMC. The validity of the inductance selection method and the inductor current balancing algorithm are confirmed by the simulation of a three phase CSMMC using PSCAD/EMTDC. The carrier phase shifted sinusoidal pulse width modulation is used as the switching technique. The performance of a converter is analyzed with both interleaved and non-interleaved carrier signals for the upper and lower arms. Results show that CSMMCs and corresponding VSMMCs have analogous features. Hence, the development on VSMMCs can be used for reference to CSMMCs and vice versa. Furthermore, the control designs for CSMMC based STATCOM are presented and verified using simulations. The obtained results of the proposed STATCOM show that the steady state and transient performance of the system are quite satisfactory. This makes the CSMMC suitable for HVDC and FACTS applications.**

***Index Terms*—Current balancing, current source modular multilevel converter, HVDC Transmission, STATCOM.**

NOMENCLATURE

VSMMC	Voltage source modular multilevel converter
SM	Submodule
HVDC	High voltage direct current
FACTS	Flexible ac transmission system
CSC	Current source converter
LCC	Line commutated converter
CSMMC	Current source modular multilevel converter
MMC	Modular multilevel converter
IGBT	Insulated-gate bipolar transistor
RB-IGBT	Reverse blocking IGBT
IGCT	Integrated gate commutated thyristor
SMES	Superconducting magnetic energy storage

I. INTRODUCTION

VOLTAGE source modular multilevel converters for high power applications have found a noticeable development in the last decade [1]-[8]. Main features of the VSMMCs include reduced harmonics, lower switching frequency, and reduced stress on each device, amongst others [1]. Moreover, because of modular structure, scalability to various power and voltage levels is easily achieved [1] and reliability can be improved by including redundant submodules in each phase [2]. These features make the VSMMCs more attractive and competitive for HVDC and FACTS applications [3]. However, the critical challenge of the voltage source converters in HVDC applications is the lack of external dc short circuit fault tolerance [8]. Various protection methods have been proposed in literature to deal with these faults [8].

On the other hand, CSCs in general are inherently tolerant to dc short-circuit faults [3]. Thyristor based LCC topology is most widely used for HVDC transmission because it is mature and well developed technology. However, the LCC based HVDC transmission system has some limitations which include: large capacitor and filter banks, lack of restoring the system without relying on external energy sources (black starting) [9] and incompatibility for the weak grid [10]-[11]. The CSCs using fully controllable switches have many advantages than LCCs. Various studies on CSCs made with self-commutating devices have been reported for HVDC and FACTS applications in [10]-[14]. The main features of CSCs using self-commutating devices are: 1) independent control of the active and reactive power, 2) it can be operated in weak grids or with passive loads, and 3) relatively small footprint because the ac side filters can be eliminated due to low harmonic distortion [10]. The CSCs using fully controllable switches requires semiconductor devices with reverse voltage blocking capability. A reverse voltage blocking device can be an IGBT in series with a diode at the expense of losses and cost [13]. RB-IGBTs and IGCTs are the other alternatives which permits reverse blocking operation [15]-[17]. By using RB-IGBT, the series diodes may be avoided and hence the losses and complexity of the converter may be reduced [15]. However, further improvements in RB-IGBT technology is needed to reduce the switching losses because of the reverse recovery effects [16]. On the other hand, aside from the higher efficiency, IGCTs are known to be very reliable and rugged with respect to over current compared to IGBTs [17]. Hence, IGCTs may be the good choice for high power applications with low voltage and high current requirements.

However, for high voltage and high current applications, requirement of series-parallel connections of large number of semiconductor devices makes these CSC topologies challenging. Multilevel CSC topologies for high power applications are reported in [18]-[20]. Main features of multilevel CSCs include reduced harmonics, lower switching frequency, and reduced stress on each device. Moreover, each module handles only a fraction of the load current which decreases the overall switching losses [19]. An MMC topology using a modified current source H-bridge cell is proposed in [21], to address the voltage scaling problem. To address the issue of both voltage and current scaling, a current source MMC using series connections of current source parallel links is proposed in [22]. However, balancing of SM inductor currents and series capacitor voltages concurrently, make the control design very complex. Moreover, detailed analytical analysis on the converter dynamics and control design are also not presented.

The main objective of this paper is to analyse in detail the

M. M. Bhesaniya and A. Shukla are with the Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai - 400076, India. (e-mail: mmb@ee.iitb.ac.in, ashukla@ee.iitb.ac.in)

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPWRD.2015.2465152, IEEE Transactions on Power Delivery

operation of a CSMMC, a dual of VSMMC, and to investigate its feasibility as a STATCOM. In CSMMC, a variable current source in each converter arm is created using parallel connected inductor SMs. This allows the direct control over output current. In addition, CSMMC is inherently dc short circuit fault tolerant and in STATCOM application, it has advantage of having reduced current harmonics compared to VSMMC [13]. This is because the harmonic source in a VSMMC system is the ac PWM output voltage; whereas, the harmonic source in a CSMMC system is the PWM output current. In STATCOM application, the current injected by the converter is a small percentage of the line current. Hence, the current harmonics are also small using CSMMC. Whereas, using VSMMC, for a small injected current, the output voltage of VSMMC is very close to the system voltage and hence, higher voltage harmonics, leading to current harmonics higher than those generated by CSMMC. Moreover, like a conventional LCC based HVDC transmission system, power reversal in CSMMC based HVDC system can be done by changing the polarity of dc-bus voltage. The power reversal action changes the dc-bus voltage polarity and the dc current direction remains the same [10]. Because of the scalability to various power and current levels, the CSMMCs are the good choice for medium voltage and high power applications such as FACTS and grid integration of wind energy. However, the inductors used as the energy storage elements in CSMMCs have the disadvantages of lower energy storage efficiency and higher conduction losses. But with the development of SMES technology, which is considered to be a very good energy storage device, some of the disadvantages of inductors can be overcome [23]-[24]. The comparisons of SMES with other energy storage devices are described in [23]. In [24], the applications of SMES are described and compared with different converter topologies.

In this paper, detail theoretical analysis of CSMMC is presented and various parameters of the converter are correlated with VSMMC. SM inductance selection method and SM inductor current balancing strategy are presented for CSMMC. Furthermore, equations are developed in dq frame to design a controller for CSMMC based STATCOM. The detailed simulation verification of a three phase standalone CSMMC and a CSMMC based STATCOM are carried out using PSCAD/EMTDC. Dynamic performances of the STATCOM during step change in capacitive mode to inductive mode and vice versa, and during ac and dc faults are evaluated.

II. CSMMC Structure and Operation

Fig. 1 shows one phase of a three phase CSMMC. Each phase of a converter consists of two arms and each arm consists of N parallel connected half bridge SMs and the arm capacitor. The inductors of the SMs act as current sources that can be inserted or bypassed in each arm of the CSMMC. This way the ac output current can be controlled by varying the number of inserted SMs in the upper and lower arms by using appropriate modulation technique. The inductor currents of all SMs are kept balanced by using a balancing technique as explained in Sec. III-B. The arm capacitor, C_{arm}, is dual to the arm inductance of a VSMMC. C_{arm} is considered to be identical for all arms of the converter. The main functions of the arm capacitor are to absorb any unbalances and harmonics generated in the arm currents [22].

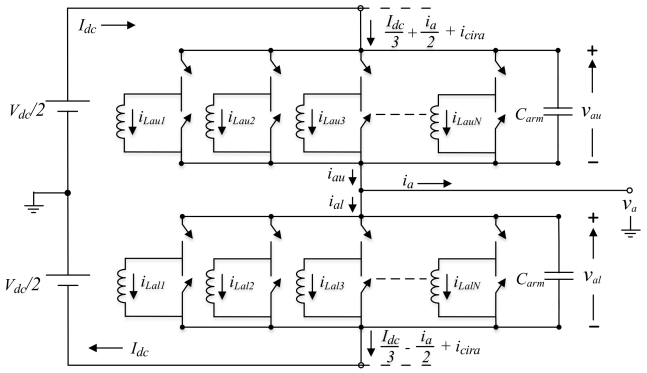

Fig. 1. Configuration of phase-a of a three phase CSMMC.

A. SM Structure and Operation

A half bridge SM of a VSMMC is shown in Fig. 2(a). This is the basic building block of a VSMMC which consists of two bidirectional switches and a capacitor. The corresponding dual, a half bridge inductor SM for a CSMMC is shown in Fig. 2(b). The controlled bidirectional switches and a capacitor are replaced with controlled reverse voltage blocking switches and an inductor respectively. In Fig. 2(b), two switches S_1 and S_2 are complimentary and their switching states are decided by using appropriate modulation technique to get the desired output current from the SM. In Fig. 2(c), S_1 is ON (S_2 is OFF), hence, the SM is inserted in the arm and the output current of the SM is effectively the inductor current. In Fig. 2(d), S_1 is OFF (S_2 is ON), hence, the SM is bypassed and the output current of the SM is zero. Nevertheless, the inductor current remains continuous through switch S_2. Hence the output current of the converter can be controlled by inserting or bypassing the SMs connected in parallel.

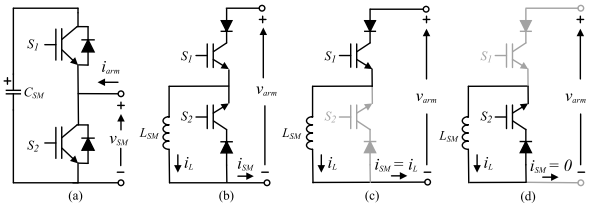

Fig. 2. (a) Half bridge capacitor SM (b) Half bridge inductor SM (c) SM inserted (d) SM bypassed.

In an SM shown in Fig. 2(b), a current path for the inductor should be provided to protect the converter against the over-voltage caused by open circuit faults. Fig. 3 shows the configuration of an SM with open circuit protection using a bypass switch T_1 and a thyristor T_2 [22]. In normal operation, switch T_1 is closed and thyristor T_2 is turned-off as shown in Fig. 3(a). When the fault is detected in the SM, thyristor T_2 is turned-on and switch T_1 is opened to bypass the faulty SM from the system as shown in Fig. 3(b). The SM inductor current remains continuous through thyristor T_2 and thus protects the SM from possible damage. Simultaneously, if the redundant SM is available then the switch T_1 of a redundant SM is closed to replace the faulty SM with a redundant SM. Hence, continuous operation of the CSMMC is ensured with increased safety and availability.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPWRD.2015.2465152, IEEE Transactions on Power Delivery

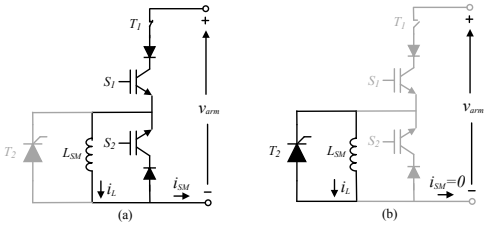

Fig. 3. Submodule open-circuit protection using thyristor (a) normal operation (b) operation during fault.

B. Assumptions

In order to simplify the mathematical analysis, some assumptions are made. These assumptions are as follows:

1) Only fundamental frequency component in the ac output waveforms is considered. This is a reasonable assumption because the number of levels in the output or the switching frequency is generally high. It will considerably simplify the analysis as well [25].
2) It is assumed that the SM inductor currents are balanced at all times to ensure stable operation of the CSMMC. This can be guaranteed by the control scheme presented in Sec. III-B, and subsequently demonstrated in Sec. V.
3) For circulating current analysis, only 2^{nd} harmonic component is considered. Aside from the 2^{nd} harmonic component, there may be other harmonics in the circulating current. However, these harmonics have a negligible impact on the accuracy of the analytical results because their amplitude is very small. This is verified using the simulation results shown in Sec. V-A.
4) For simplicity, balanced grid voltages have been assumed and hence only positive sequence components of the three phase voltages and currents are considered. Under unbalanced grid conditions, not only the positive sequence components, but also the negative sequence components are taken into considerations [26].

C. Analysis and Operation of CSMMC

To analyse the operation of a converter, phase-a of a three phase CSMMC, shown in Fig. 1, is considered. If the upper switch in an SM is ON, the output of the SM is equal to the corresponding inductor current; otherwise, it is zero. Hence, each arm of the CSMMC represents a controllable current source and the desired output current is obtained by varying the number of inserted and bypassed SMs in each arm. The ac output current i_a and phase voltage v_a are defined as

$$i_a = \hat{I}_a \, sin\omega_0 t, \quad v_a = \hat{V}_a \, sin(\omega_0 t + \phi). \tag{1a,b}$$

Here, $\hat{I}_a$ and $\hat{V}_a$ are the peak values of the output current and voltage respectively, ω_0 is the fundamental frequency and ϕ is the load phase angle. The effective inductances of upper and lower arms of phase-a, are given by

$$L_{au} = L_{SM}/N_{au}, \quad L_{al} = L_{SM}/N_{al}. \tag{2a,b}$$

Here, N_{au} and N_{al} are the number of SMs inserted in upper and lower arms respectively and L_{SM} is the SM inductance. Using KCL, the total output currents of upper and lower arm SMs of phase-a in Fig. 1 can be expressed by

$$i_{Lau} = \sum_{j=1}^{N_{au}} i_{Lauj}, \quad i_{Lal} = \sum_{j=1}^{N_{al}} i_{Lalj}. \tag{3a,b}$$

Note that i_{Lauj}, $j = 1, .., N_{au}$ and i_{Lalj}, $j = 1, .., N_{al}$, are the currents of inserted SMs in upper and lower arm respectively. Using (3), the upper and lower arm currents i_{au} and i_{al} in Fig. 1 are defined by

$$i_{au} = C_{arm}\frac{dv_{au}}{dt} + i_{Lau}, \quad i_{al} = C_{arm}\frac{dv_{al}}{dt} + i_{Lal} \tag{4a,b}$$

where, v_{au} and v_{al} are the upper and lower arm voltages respectively. The arm currents, i_{au} and i_{al}, consists of three components: 1) the dc current, $I_{dc}/3$, which is responsible to keep the arm energized or to maintain the SM inductor currents around their reference value; 2) half of the ac side current; and 3) the circulating currents which circulate within the three phases of the converter. Hence, i_{au} and i_{al} can also be written as

$$i_{au} = \frac{I_{dc}}{3} + \frac{i_a}{2} + i_{cira}, \quad i_{al} = \frac{I_{dc}}{3} - \frac{i_a}{2} + i_{cira} \tag{5a,b}$$

where i_{cira} is the circulating current in phase-a. Depending upon the switching technique, the circulating current contains any number of harmonic components. Therefore, in steady state, i_{cira} can be given by the general expression

$$i_{cira} = \sum_{n=1}^{\infty} i_{ciran} \, sin(n\omega_0 t + \phi_n). \tag{6}$$

If the circulating currents, i_{cirp}, $p = a, b, c$, of the three phases have equal magnitude and phase difference of $2\pi/3$, then,

$$i_{cira} + i_{cirb} + i_{circ} = 0. \tag{7}$$

Therefore, the circulating currents have no effect outside the converter either on the ac or dc side. However, they have a significant impact on the rating of converter components and the losses of the converter. Hence, they should be kept as close to zero as possible.

The ac side current of phase-a can be obtained by subtracting (5b) from (5a), that is

$$i_a = i_{au} - i_{al}. \tag{8}$$

Using KVL, the ac voltage of phase-a in Fig. 1 is defined by

$$v_a = -v_{au} + V_{dc}/2 \tag{9}$$

or
$$v_a = v_{al} - V_{dc}/2 \tag{10}$$

or
$$v_a = (v_{al} - v_{au})/2. \tag{11}$$

The dc link voltage is then derived from (9) and (10)

$$V_{dc} = v_{au} + v_{al}. \tag{12}$$

Using (5a) or (5b) for all the three phases, the total dc link current in terms of i_{pu} or i_{pl}, $p = a, b, c$ is expressed as

$$I_{dc} = i_{au} + i_{bu} + i_{cu} \quad \text{or} \quad I_{dc} = i_{al} + i_{bl} + i_{cl}. \tag{13}$$

Substituing (4) in (8) yields

$$i_a = C_{arm}\frac{d}{dt}(v_{au} - v_{al}) + i_{Lau} - i_{Lal}. \tag{14}$$

Inserting (11) in (14) gives

$$i_a = -2C_{arm}\frac{dv_a}{dt} + i_{Lau} - i_{Lal}. \tag{15}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPWRD.2015.2465152, IEEE Transactions on Power Delivery

It is clear from (15) that i_{Lau} and i_{Lal} should be controlled to get the desired output current. To specify the reference currents i_{Lau} and i_{Lal}, the harmonic and circulating currents are ignored. Hence, using (1a) and (4)-(5), the reference currents of the upper and lower arms of phase-a in time domain are expressed as

$$i_{Lau} = \frac{I_{dc}}{3} + \frac{\hat{I}_a}{2} sin\omega_0 t = \frac{I_{dc}}{3}[1 + m_i sin\omega_0 t] \tag{16}$$

$$i_{Lal} = \frac{I_{dc}}{3} - \frac{\hat{I}_a}{2} sin\omega_0 t = \frac{I_{dc}}{3}[1 - m_i sin\omega_0 t] \tag{17}$$

where m_i is the modulation index, defined by $m_i = \frac{3\hat{I}_a}{2I_{dc}}$.

Similarly, substituting (1b) in (9) and (10), the voltages in each arm of phase-a in time domain are given by

$$v_{au} = \frac{V_{dc}}{2}[1 - m_v sin(\omega_0 t + \phi)] \tag{18}$$

$$v_{al} = \frac{V_{dc}}{2}[1 + m_v sin(\omega_0 t + \phi)] \tag{19}$$

where m_v is defined by $m_v = \frac{2\hat{V}_a}{V_{dc}}$. Using (16) to (19), the instantaneous power delivered to the upper and lower arms of phase-a of the converter are derived as

$$\begin{aligned} p_{au} &= v_{au} \times i_{Lau} \\ &= \frac{V_{dc}I_{dc}}{6}[1 + m_i sin\omega_0 t - m_v sin(\omega_0 t + \phi) - \\ &\quad \frac{m_i m_v}{2}(cos\phi - cos(2\omega_0 t + \phi))] \end{aligned} \tag{20}$$

$$\begin{aligned} p_{al} &= v_{al} \times i_{Lal} \\ &= \frac{V_{dc}I_{dc}}{6}[1 - m_i sin\omega_0 t + m_v sin(\omega_0 t + \phi) - \\ &\quad \frac{m_i m_v}{2}(cos\phi - cos(2\omega_0 t + \phi))]. \end{aligned} \tag{21}$$

The internal energy of phase-a can be calculated by summing and integrating (20) and (21), that is,

$$E_a = \frac{V_{dc}I_{dc}}{6}[2t - m_i m_v cos\phi t + \frac{m_i m_v}{2\omega_0}(sin(2\omega_0 t + \phi))]. \tag{22}$$

In steady state, if the losses in the converter are neglected then the dc component of the energy should not appear in the arms. Otherwise the energy in the SM inductors will increase or decrease continuously. Hence,

$$2t - m_i m_v cos\phi t = 0 \quad \text{or} \quad m_i m_v = 2/cos\phi. \tag{23}$$

Substituting $m_i m_v$ from (23) in (22), one get the alternating energy in the converter phase

$$E_a = \frac{V_{dc}I_{dc}}{6\omega_0 cos\phi} sin(2\omega_0 t + \phi). \tag{24}$$

Eq. (24) shows that the energy in the converter arms fluctuates at twice the fundamental frequency. This is in line with the 2^{nd} harmonic current in circulating current of VSMMC [27].

D. Circulating Current Analysis

The arm current of the CSMMC is coupled to the dc side of the SM by the switching actions, thereby generating ripple current in the SM inductor. This ripple current is reflected to the SM output terminal. The sum of the ripple component of all the SMs within one phase forms the circulating current. Hence, the circulating current component in the arm current is influenced by the inductor ripple current. Since the size of the SM inductor is appropriately selected to limit the ripple current as explained in Sec. II-E, the circulating current is also limited. On the other hand, in VSMMC, the circulating current is caused due to the sum of ripple voltages of all the SMs within one phase [25]. This circulating current is limited by the arm inductors. However, the value of arm inductors should not be very large, and hence an additional control effort for limiting the circulating current is required in VSMMC [27].

As shown in (24), the energy in the converter arms fluctuates at twice the fundamental frequency and therefore, the most significant component in the circulating current will be the 2^{nd} harmonic. To solve for the amplitude and phase of this 2^{nd} harmonic circulating current, the early assumptions of the arm currents in (16)-(17) are revised and the 2^{nd} harmonic circulating component is supposed to exist in the arm currents. That is,

$$i_{au} = \frac{I_{dc}}{3} + \frac{\hat{I}_a}{2} sin\omega_0 t + \hat{I}_{2f} sin(2\omega_0 t + \phi_2) \tag{25}$$

$$i_{al} = \frac{I_{dc}}{3} - \frac{\hat{I}_a}{2} sin\omega_0 t + \hat{I}_{2f} sin(2\omega_0 t + \phi_2) \tag{26}$$

where, $\hat{I}_{2f}$ and ϕ_2 denote the amplitude and phase of the 2^{nd} harmonic circulating current. Using (18)-(19) and (25)-(26), the expressions for the revised instantaneous power delivered to the upper and lower arms of phase-a are derived as

$$p'_{au} = p_{au} + \frac{\hat{I}_{2f}V_{dc}}{2} sin(2\omega_0 t + \phi_2)[1 - m_v sin(\omega_0 t + \phi)] \tag{27}$$

$$p'_{al} = p_{al} + \frac{\hat{I}_{2f}V_{dc}}{2} sin(2\omega_0 t + \phi_2)[1 + m_v sin(\omega_0 t + \phi)]. \tag{28}$$

The alternating energy in phase-a is then obtained by summing and integrating (27) and (28), and inserting (23). That is,

$$E_a = \frac{V_{dc}I_{dc}}{6\omega_0 cos\phi} sin(2\omega_0 t + \phi) - \frac{V_{dc}\hat{I}_{2f}}{2\omega_0} cos(2\omega_0 t + \phi_2). \tag{29}$$

If the upper and lower arms of CSMMC with N SMs per arm, are controlled such that at any instant $N_{au} + N_{al} = N$, and the SM inductor currents are balanced, then the average SM inductor current i_L is expressed as

$$i_L = (i_{au} + i_{al})/N. \tag{30}$$

Adding (25) in (26) and inserting (30) gives

$$i_L = \frac{2\, I_{dc}}{3\, N} + \frac{2\, \hat{I}_{2f}}{N} sin(2\omega_0 t + \phi_2). \tag{31}$$

Since, N SMs are inserted in a phase at any instant, the total energy E_{La} in phase-a is given by

$$\begin{aligned} E_{La} &= N\frac{1}{2}L_{SM}\, i_L^2 \\ &= \frac{2I_{dc}L_{SM}I_{dc}^2}{9N} + \frac{4L_{SM}I_{dc}\hat{I}_{2f}}{3N} sin(2\omega_0 t + \phi_2) + \\ &\quad \frac{2L_{SM}\hat{I}_{2f}^2}{N} sin^2(2\omega_0 t + \phi_2). \end{aligned} \tag{32}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPWRD.2015.2465152, IEEE Transactions on Power Delivery

Comparing 2^{nd} harmonic component in (29) and (32) gives

$$\frac{V_{dc}I_{dc}}{6\omega_0 cos\phi}sin(2\omega_0 t+\phi) - \frac{V_{dc}\hat{I}_{2f}}{2\omega_0}cos(2\omega_0 t+\phi_2) = \frac{4L_{SM}I_{dc}\hat{I}_{2f}}{3N}sin(2\omega_0 t+\phi_2). \quad (33)$$

By solving (33), the amplitude $\hat{I}_{2f}$ and the phase ϕ_2 for the 2^{nd} harmonic circulating current are obtained as

$$\hat{I}_{2f} = \frac{NV_{dc}I_{dc}}{cos\phi\sqrt{(8\omega_0 L_{SM}I_{dc})^2+(3NV_{dc})^2}} \quad (34)$$

$$\phi_2 = \phi - arctan(3NV_{dc},\, 8\omega_0 L_{SM}I_{dc}). \quad (35)$$

Eq. (34) shows that under given operating condition, the 2^{nd} harmonic circulating current is limited by the SM inductor, which is verified using the study results shown in Sec. V-A.

E. SM Inductance Selection

The stored energy E_L in an inductor of each SM of CSMMC changes with time because the energy in the arm is fluctuating as shown by (24). This results in the current ripples in SM inductors. The current ripple in SM inductors depends on the size of the SM inductor L_{SM} and the energy-power ratio $E(S)$. Here, $E(S)$ signifies the energy storage requirements in the converter in terms of total energy storage per transferred MVA [28]. Since, $E(S)$ is independent of the specific energy storage device [29], it can be assumed to be same as that used for SM capacitance selection for VSMMC. Typically $E(S)$ is in the range of 10 kJ/MVA to 50 kJ/MVA depending upon the converter application [4].

The stored energy, E_L, in an SM inductor is expressed as

$$E_L = \frac{1}{2}L_{SM}\, i_L^2. \quad (36)$$

Using (36), the total stored energy E in six arms of a three phase CSMMC with rated power S is obtained by

$$E = 6\, N\, E_L \quad (37)$$

or

$$S\, E(S) = 6\, N\, \frac{1}{2}L_{SM}\, i_L^2. \quad (38)$$

The SM inductance L_{SM} is then calculated as follows:

$$L_{SM} = \frac{S\, E(S)}{3\, N\, i_L^2}. \quad (39)$$

Equation (39) confirms the duality in selection of SM inductance with that of SM capacitance selection given in [5].

Alternatively, L_{SM} can also be derived as a function of inductor current ripple by considering the energy variation in the arm. Multiplying (36) with the number of SMs in an arm gives the stored energy in each arm. That is,

$$E_{arm} = \frac{1}{2}NL_{SM}\, i_L^2. \quad (40)$$

The current in each SM will vary with time as the inductors are charged and discharged. Consequently, the energy variation in each arm can be expressed as

$$E_{arm} + \frac{\Delta E}{2} = \frac{1}{2}\, N\, L_{SM}\, (i_L(1+\Delta i_L))^2 \quad (41)$$

and

$$E_{arm} - \frac{\Delta E}{2} = \frac{1}{2}\, N\, L_{SM}\, (i_L(1-\Delta i_L))^2. \quad (42)$$

where, ΔE represents the peak to peak energy variation in the arm and Δi_L is the per unit current ripple in SM inductor for any given operating point. The inductance of the SM inductors can then be calculated by subtracting (42) from (41) and solving for L_{SM}. Accordingly,

$$L_{SM} = \frac{\Delta E}{2\, N\, i_L^2\, \Delta i_L}. \quad (43)$$

Equation (43) also confirms the duality in selection of SM inductance with that of SM capacitance selection given in [30].

III. CSMMC Control

In CSMMC multiple SMs are connected in parallel in each arm. Hence to get the desired output current, it is required to insert or bypass a certain number of SMs in each arm at any point of time and the current through all the SMs should be balanced. This is done by using appropriate switching and balancing technique as explained below.

A. Switching Technique

To synthesize a multi-level output current waveform at the ac side of the CSMMC, the carrier phase shifted sinusoidal pulse width modulation (CPS-SPWM) scheme is used here. CPS-SPWM is most commonly used modulation strategy for modular multilevel converters as it has some distinctive features. The main feature of the CPS-SPWM is that the power handled by each SM of the same arm is evenly distributed [6]. Hence, using CPS-SPWM the inductor current balancing control can be easily achieved in CSMMC. The SM is inserted or bypassed based on the switching state produced from the intersection of sinusoidal modulating signal and triangular carrier signal. Moreover, two options exists with CPS-SPWM: 1) non-interleaved switching; and 2) interleaved switching [7].

In non-interleaved switching, converter with N SMs per arm requires N triangular carriers with a switching frequency of f_{sw}, while each triangular carrier have phase difference of $2\pi/N$. The triangular carriers for upper and lower arms of converter are same. The reference signals of upper and lower arms are phase shifted by π radians.

On the other hand, in interleaved switching, converter with N SMs per arm requires $2N$ triangular carriers with a switching frequency of f_{sw}, while each triangular carrier have phase difference of π/N. Hence, the number of carrier signals required are twice the number of SMs per arm. However, the phase difference between two consecutive triangular carriers of the same arm will be $2\pi/N$.

B. Inductor Current Balancing

In ideal condition, the current through each SM inductor of a CSMMC is given by (31). However, due to different electrical parameters of the SMs, the current through the SM inductors tend to be out of balance. Hence, a sorting based algorithm is proposed here for SM inductor current balancing in a CSMMC. Balancing of inductor currents in CSMMC is analogous to the balancing of capacitor voltages in VSMMC. The modulation technique, as described in Sec. III-A, determines the number of SMs to be inserted or bypassed in the upper and lower arms of the converter. In order to keep the inductor currents balanced, a sorting based rule for inserting or

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPWRD.2015.2465152, IEEE Transactions on Power Delivery

bypassing of each SM is followed. The objective of the sorting strategy is to charge or discharge the correct SM inductor. This is possible because the output current levels generated in CSMMC depends upon the number of SMs inserted in upper and lower arms and not by the specific order the SMs are inserted. Table I describes one of the possible switching states with non-interleaved switching for each current level in phase-a of three phase five level CSMMC. A block diagram of the SM inductor current balancing algorithm in a CSMMC for phase-a is shown in Fig. 4.

The number of SMs to be inserted in upper and lower arms of phase-a are determined by the comparison of the sinusoidal modulating signals and triangular carrier signals, as shown in Fig. 4. For the specified number of SMs to be inserted or bypassed, there are several combinations of SMs. The selection of the proper combination is done based on the values of SM inductor currents as well as the polarity of arm voltage. When the SM is inserted, the inductor current increases (decreases) if the voltage across SM is positive (negative). This fact is used for the SM inductor current balancing. The switching signals generated from this algorithm are given to the CSMMC. Moreover, as can be observed in the diagram of Fig. 4, sorting is done only when the SM is to be inserted or bypassed to reduce the switching losses.

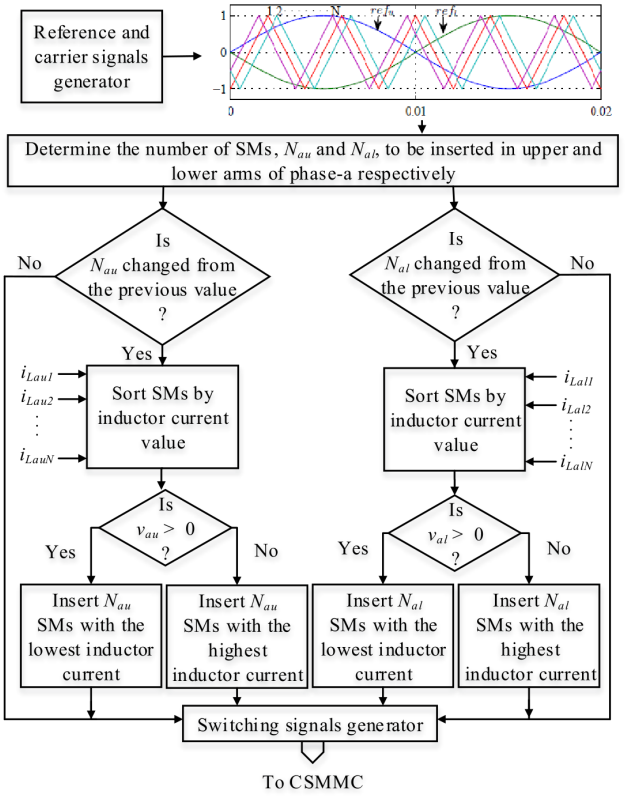

Fig. 4. Block diagram of the indicator current balancing algorithm including CPS-SPWM for phase-a of a three phase CSMMC.

IV. CSMMC BASED STATCOM

The circuit configuration of a CSMMC based STATCOM is shown in Fig. 5. The STATCOM is connected to the grid through a coupling transformer. In Fig. 5, i_{Lau} and i_{Lal} represent controllable current sources, whose instantaneous value depends on the number of inserted and bypassed SMs in each arm. C_f is the capacitance of the harmonic filter. L_{dc} is the dc link reactor used to reduce the dc current ripple.

TABLE I
ONE OF THE POSSIBLE SWITCHING STATES FOR EACH CURRENT LEVEL IN PHASE-a OF A THREE PHASE FIVE LEVEL CSMMC

SM_{au1}	SM_{au2}	SM_{au3}	SM_{au4}	i_{au}	i_{al}	i_a
1	1	1	1	$2I_{dc}/3$	0	$2I_{dc}/3$
1	1	1	0	$I_{dc}/2$	$I_{dc}/6$	$I_{dc}/3$
1	1	0	0	$I_{dc}/3$	$I_{dc}/3$	0
1	0	0	0	$I_{dc}/6$	$I_{dc}/2$	$-I_{dc}/3$
0	0	0	0	0	$2I_{dc}/3$	$-2I_{dc}/3$

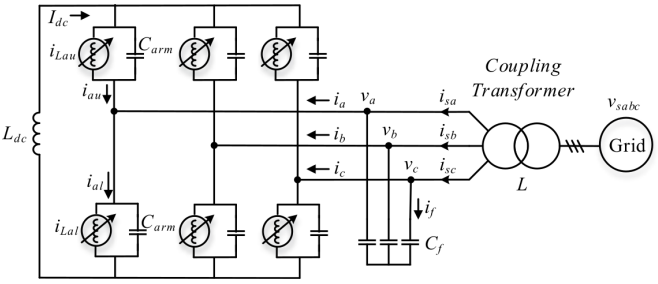

Fig. 5. Configuration of CSMMC based STATCOM

A. Controller Design

The control objectives for the system of Fig. 5 are to provide the required reactive power compensation Q_{ref} to the grid and to regulate the dc-link current I_{dc}. The controller is implemented based on current mode control in synchronous dq frame as shown in Fig. 6. In this approach, the CSMMC line current is regulated by the inner current control loop. The reactive power and dc link current are controlled by the outer current control loop.

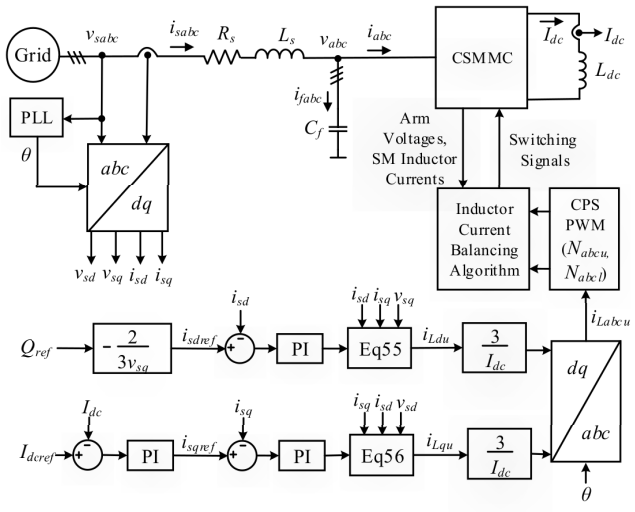

Fig. 6. Diagram of CSMMC based STATCOM control system

The dynamic equations of phase-a in abc frame for the system of Fig. 6 are expressed as

$$i_a = 2C_{arm}\frac{dv_a}{dt} - i_{Lau} + i_{Lal} \tag{44}$$

$$i_{sa} = i_a + C_f\frac{dv_a}{dt} \tag{45}$$

$$v_{sa} = v_a + R_s i_{sa} + L_s\frac{di_{sa}}{dt}. \tag{46}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPWRD.2015.2465152, IEEE Transactions on Power Delivery

Here, (44) is obtained using (15) by considering the direction of the current as shown in Fig. 6. Note that L_s and R_s in (46) represent the leakage inductance and resistance of the coupling transformer. These equations are valid for all the three phases. In (44), either the upper or lower arm current is selected to be the output of the controller because the upper and lower arm currents are phase shifted by π radians. Solving (16), (17) and (44), the converter line current in terms of the upper arm current is expressed as

$$i_a = 2C_{arm}\frac{dv_a}{dt} - 2i_{Lau} + \frac{2I_{dc}}{3}. \tag{47}$$

Eqs. (45), (46) and (47) are transformed to the synchronous dq frame using the transformation T given by

$$T = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}. \tag{48}$$

Here, the d-axis is aligned to the grid voltage vector such that the d-axis component of grid voltage $v_{sd} = 0$. The phase locked loop (PLL) is used to detect the phase θ of the grid voltage. For simplicity, a balanced grid voltage is assumed; hence the zero-sequence component is zero. Thus, the dq transformation of (47), (45) and (46) results in

$$i_d = 2C_{arm}\frac{dv_d}{dt} + 2\omega C_{arm}v_q - 2i_{Ldu} \tag{49}$$

$$i_q = 2C_{arm}\frac{dv_q}{dt} - 2\omega C_{arm}v_d - 2i_{Lqu} \tag{50}$$

$$i_{sd} = i_d + C_f\frac{dv_d}{dt} + \omega C_f v_q \tag{51}$$

$$i_{sq} = i_q + C_f\frac{dv_q}{dt} - \omega C_f v_d \tag{52}$$

$$v_{sd} = R_s i_{sd} + L_s\frac{di_{sd}}{dt} + \omega L_s i_{sq} + v_d \tag{53}$$

$$v_{sq} = R_s i_{sq} + L_s\frac{di_{sq}}{dt} - \omega L_s i_{sd} + v_q. \tag{54}$$

In steady state, all derivatives can be set to zero. Thus, solving (49)-(54) and using the output of the inner PI controllers, dq components of the upper arm reference current i_{Ldu} and i_{Lqu} in steady state are determined as

$$\begin{aligned} i_{Ldu} =& PI(i_{sdref} - i_{sd}) - \frac{1}{2}((1 - \omega^2 L_s(C_f + 2C_{arm}))i_{sd} - \\ & \omega(C_f + 2C_{arm})v_{sq} + \omega(C_f + 2C_{arm})R_s i_{sq}) \end{aligned} \tag{55}$$

$$\begin{aligned} i_{Lqu} =& PI(i_{sqref} - i_{sq}) - \frac{1}{2}((1 - \omega^2 L_s(C_f + 2C_{arm}))i_{sq} + \\ & \omega(C_f + 2C_{arm})v_{sd} - \omega(C_f + 2C_{arm})R_s i_{sd}). \end{aligned} \tag{56}$$

Note that the reference current i_{sdref} is generated based on commanded reactive power Q_{ref} in outer control loop. With the aligned synchronous frame, d-axis component of grid voltage $v_{sd} = 0$. Therefore, the reactive power output to the grid can be expressed as follows:

$$Q_{ref} = -\frac{3}{2}v_{sq}i_{sdref}. \tag{57}$$

To obtain i_{sqref}, the dc current controller is employed as shown in Fig. 6. Finally, the reference arm currents i_{Ldu} and i_{Lqu} obtained from (55) and (56) are normalized within the range $[-1, 1]$, and transformed back to the abc frame to get the upper arm reference currents i_{Lpu}, $p = a, b, c$, as shown in Fig. 6. The lower arm reference currents i_{Lpl}, $p = a, b, c$ in respective phase are shifted by π radians. Switching signals are then generated using CPS-SPWM and inductor current balancing technique. These switching signals are given to the CSMMC. Depending on the switching singles, the CSMMC generates the desired output current by inserting/bypassing the SMs in each arm.

V. Case Studies

To demonstrate the operation of the CSMMC, the simulation of a three phase CSMMC is carried out by using PSCAD/EMDTC. The inductance selection method described in Sec. II-E is used for the selection of SM inductance. CPS-PWM strategy of Sec. III-A in conjunction with the inductor current balancing algorithm of Sec. III-B are used to control the operation of CSMMC. Moreover, to verify the operation and control of CSMMC as a STATCOM, simulation results of a grid connected CSMMC of Fig. 5 are presented.

A. Standalone CSMMC

Parameters of a converter used for the simulation of a standalone CSMMC are shown in Table II. The SM inductance of CSMMC is evaluated using (39) for energy power ratio $E(S) = 30$ kJ/MVA and the rated power $S = 10$ MVA. This ensures the ripple of the SM inductor current within the rage of $\pm 10\%$.

TABLE II
CSMMC Parameters for Simulation

DC Link Voltage	$V_{dc} = 3$ kV
Converter Parameters	$N = 4$, $L_{SM} = 100$ mH, $C_{arm} = 50$ μF, $f_{sw} = 1$ kHz
Load	$f_0 = 50$ Hz, $L = 3$ mH, $cos\phi = 0.9$

Simulation results of phase-a of a standalone CSMMC are shown in Fig. 7. CPS-SPWM switching from interleaved to non-interleaved is done at $t = 1$ s. Fig. 7(a) shows the differential current ($i_{La} = i_{Lau} - i_{Lal}$) and the ac side current. It can be seen that the ac side current does not have a dc component. Arm capacitor of CSMMC also acts as a filter hence, the output current contains less harmonics which can be further reduced either by using the ac side filter or by increasing the number of SMs in an arm. Fig. 7(b) shows the arm voltages and ac side voltage which are analogous to the arm currents and ac side current in VSMMC. Fig. 7(c) shows the circulating current between the phases. Since the circulating current cannot be measured directly, it is calculated using (5). It can be observed that the 2^{nd} harmonic component in circulating current is predominant. Fig. 7(d) shows the SM inductor currents in the upper and lower arms. It verifies the capability of the proposed inductor current balancing strategy to regulate and maintain the SM inductor currents at their nominal values. Fig. 7(d) also shows that the proposed inductance selection method ensures the ripple of the SM inductor current within the rage of $\pm 10\%$.

Moreover, the simulation results manifest clearly that the number of levels in output currents with interleaved switching are more than with non-interleaved switching. But this also

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPWRD.2015.2465152, IEEE Transactions on Power Delivery

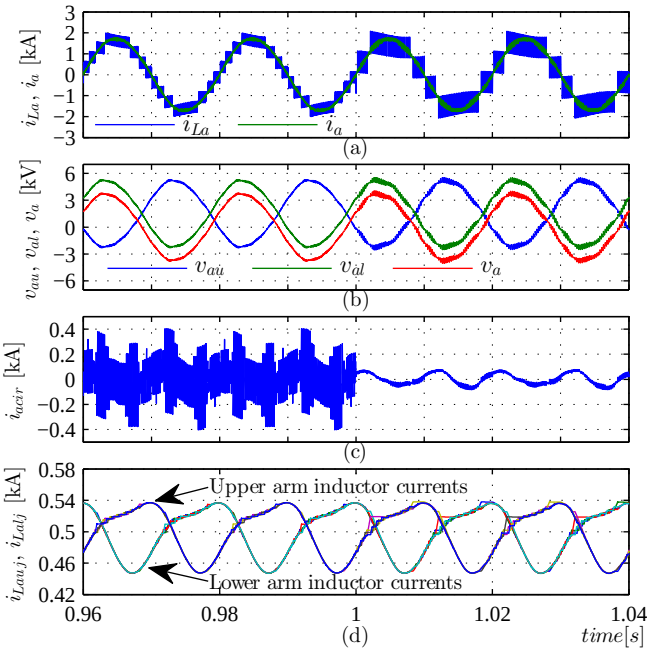

Fig. 7. Simulated waveforms of phase-a of a standalone CSMMC with interleaved switching for $t < 1$ s, and non-interleaved switching for $t \geq 1$ s. (a) Calculated i_{La} and output current (b) Arm voltages and output voltage (c) Circulating current (d) Inductor currents in upper and lower arms.

increases ripple in circulating currents which affects the rating of the converter components and the losses in the converter. Hence, non-interleaved switching is preferred and considered further for the simulation of CSMMC based STATCOM. In VSMMC also non-interleaved switching is preferred due to the same reason.

Fig. 8 shows the spectrum of the arm current and the circulating current with non-interleaved switching. It can be observed from Fig. 8(a) that the circulating current is limited due the SM inductance. Fig. 8(b) demonstrates that the most significant component in the circulating current is the 2^{nd} harmonic and the amplitudes of the other harmonics are very small. Fig. 9 shows the comparison of simulation results with the analytically calculated results of 2^{nd} harmonic circulating current with different values of SM inductance. It shows that the analytically calculated results are very close to the simulation results, which validates the analytical procedure presented in the paper.

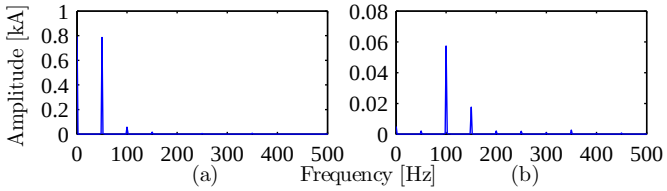

Fig. 8. Spectrum of (a) arm current and (b) circulating current.

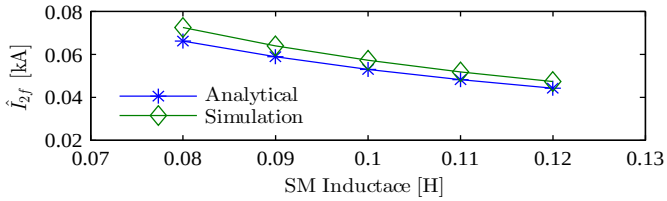

Fig. 9. Comparison between the simulated and analytically calculated values of 2^{nd} harmonic circulating current with different values of SM inductance.

B. CSMMC based STATCOM

System parameters for the simulation of CSMMC based STATCOM are shown in Table III. The SM inductance of CSMMC is evaluated using (39) for energy power ratio $E(S) = 30$ kJ/MVA and the rated power $S = 50$ MVA.

TABLE III
SYSTEM PARAMETERS FOR CSMMC BASED STATCOM

Grid Voltage/Frequency	$V_p = 115$ kV (line-line RMS), $f_0 = 50$ Hz
Coupling Transformer	115/11 kV, 50 MVA, $L_s = 0.16$ pu
Converter Parameters	$N = 4$, $S = 50$ MVA, $L_{SM} = 281$ mH, $C_{arm} = 15$ μF, $f_{sw} = 1$ kHz
DC-link reactor	$L_{dc} = 50$ mH
Filter Capacitance	$C_f = 75$ μF

Simulation results during transition from capacitive to inductive mode of operation are shown in Fig. 10. The reactive power reference Q_{ref} is varied from -40 MVAr (capacitive) to $+20$ MVAr (inductive) as shown in in Fig. 10(a). The grid side current and voltage in dq frame are shown in Fig. 10(b) and Fig. 10(c) respectively. It can be seen from the results that the settling time of the control system is less than 50 ms. The voltage waveform of phase-a and associated line current waveform on the secondary side (11 kV) of a coupling transformer are shown in Fig. 10(d). These waveforms show the transient free and fast response of the control system. Fig. 10(e) and Fig. 10(f) show the output line current of converter and the filter capacitor current respectively.

Similarly, the simulation results during transition from $+20$ MVAr (inductive) to -40 MVAr (capacitive) are shown in Fig. 11. The results in both the mode of operation show the smooth and fast response of the control system. Fig. 12(a) shows the SM inductor currents in upper arm during capacitive and inductive mode of operations. It shows the capability of the proposed inductor current balancing strategy to control the SM inductor currents in both the operating modes. Fig. 12(b) shows the dc link current I_{dc} which is maintained at 4 kA.

A dc short circuit fault is tested to show the dc fault tolerance capability of the CSMMC and results are presented in Fig. 13. The CSMMC is operating in a capacitive mode supplying 40 MVAr to the grid. The dc link is short circuited at $t = 11.0$ s, for a duration of 0.2 s. It can be observed that the grid side currents and voltages are undisturbed and CSMMC continues to supply the commanded reactive power to the grid. The dc link inductor is used to suppress the dc-current ripples in normal operation. During the dc fault it is shorted, and hence the dc-current ripples increase slightly.

The case for three phase to ground fault through impedance of 75Ω with $X/R = 1$ is simulated and results are presented in Fig. 14. The fault occurs at $t = 7.0$ s, for a duration of 0.5 s. It can be observed that the reactive power exchange by the converter with the grid remains the same despite of reduction in grid voltage. The grid voltage can be maintained at desired level by operating the converter in ac voltage control mode.

VI. CONCLUSION

The detailed analytical analysis of a CSMMC and its application as a STATCOM have been presented. In CSMMC, it is important to select SM inductance appropriately because

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPWRD.2015.2465152, IEEE Transactions on Power Delivery

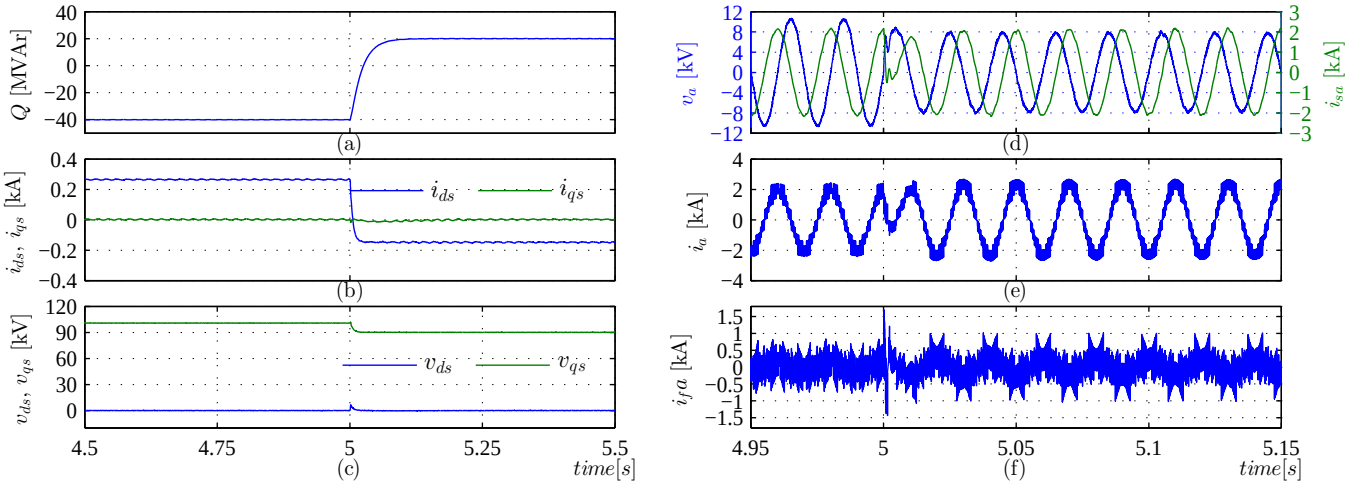

Fig. 10. Simulation results of STATCOM during transition from capacitive to inductive mode of operation at $t = 5$ s. (a) Reactive power (b) dq components of a gird current (c) dq components of a gird voltage (d) Phase voltage and current (11kV side) (e) Output current of converter (before filter) (f) Filter current.

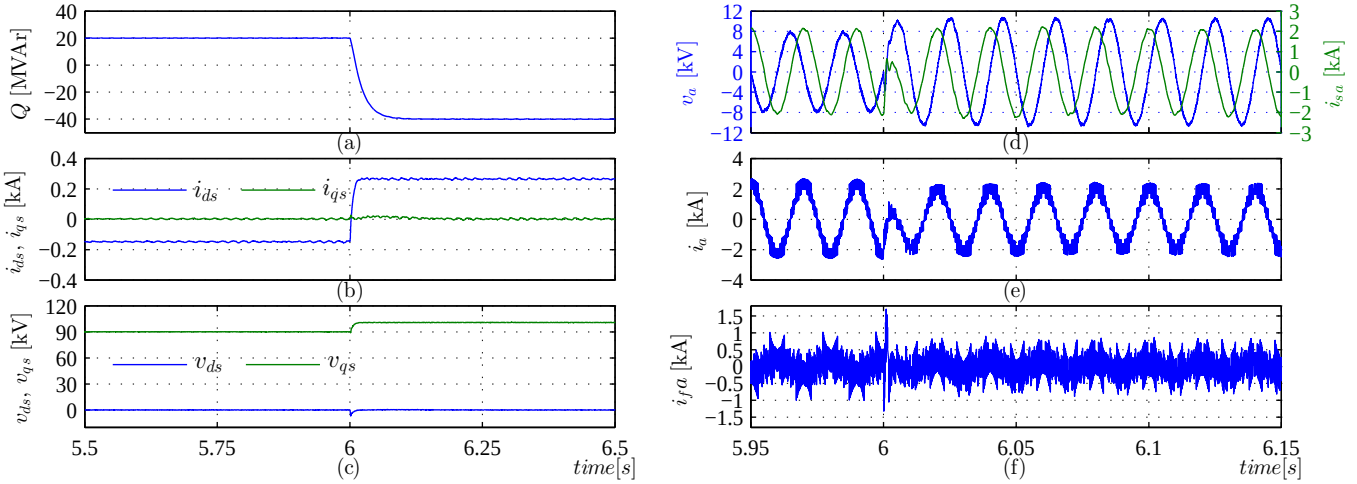

Fig. 11. Simulation results of STATCOM during transition from inductive to capacitive mode of operation at $t = 6$ s. (a) Reactive power (b) dq components of a gird current (c) dq components of a gird voltage (d) Phase voltage and current (11kV side) (e) Output current of converter (before filter) (f) Filter current.

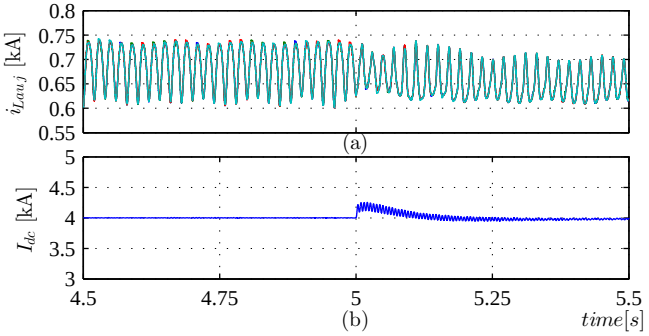

Fig. 12. (a) SM inductor currents in upper arm during transition from capacitive to inductive mode of operation at $t = 5$ s. (b) DC link current.

it strongly influences the inductor current ripple. Hence, the method for SM inductance selection is proposed. To maintain the SM inductor currents at their reference values, a sorting based algorithm for inductor current balancing has been proposed. The control strategy in dq frame is presented for the CSMMC based STATCOM. The effectiveness of these methods and the dynamic performance of the designed controllers for the CSMMC based STATCOM is investigated using PSCAD/EMTDC simulations under various operating conditions. The obtained results confirm that the properties of CSMMC correlate with the corresponding VSMMC. Hence

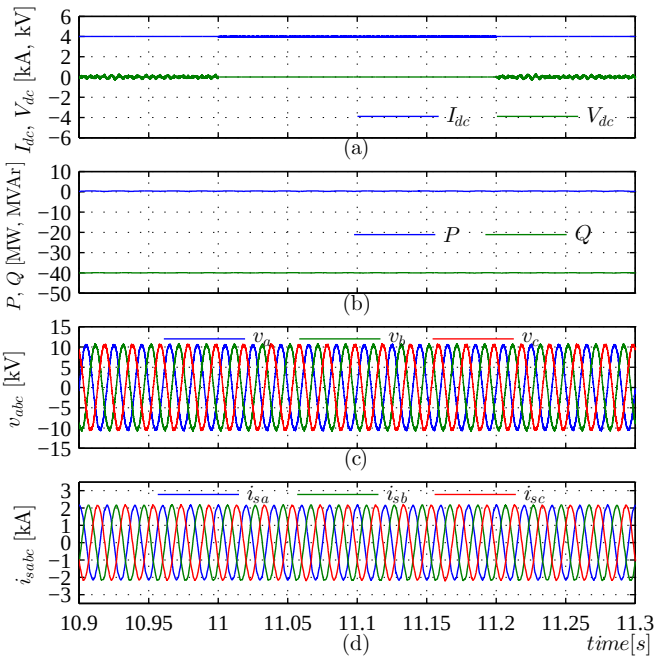

Fig. 13. Simulation results of STATCOM during DC fault at $t = 11$ s, for a duration of 0.2 s. (a) DC link current and voltage (b) Active and reactive power (c) and (d) Three phase voltages and currents (11kV side) .

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPWRD.2015.2465152, IEEE Transactions on Power Delivery

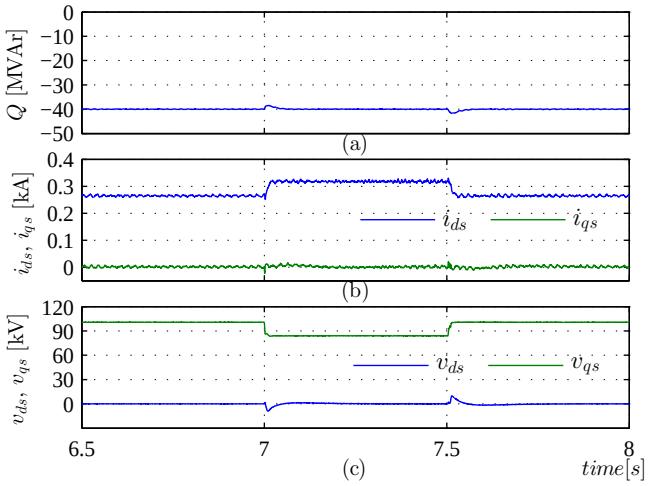

Fig. 14. Simulation results of STATCOM during AC fault on gird side at $t = 7$ s, for a duration of 0.5 s. (a) Reactive power (b) dq components of a gird current (c) dq components of a gird voltage.

the developments on CSMMCs and VSMMCs can be used as reference for each other. The study demonstrates that the proposed inductance selection method ensures the ripple of the SM inductor current within the rage. The study also shows that the proposed inductor current balancing strategy can effectively provide current balancing for the CSMMC inductors. Moreover, it is demonstrated that the CSMMC based STATCOM, using appropriately designed controllers, provides the desired dynamic response under different operating conditions. Hence, CSMMC can be considered as the potential candidate for HVDC and FACTS applications.

REFERENCES

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Power Tech Conf.,* Bologna, vol. 3, June 2003.

[2] B. Li, Y. Zhang, R. Yang, R. Xu, D. Xu, and W. Wang, "Seamless transition control for modular multilevel converters when inserting a cold-reserve redundant submodule," *IEEE Trans. Power Electron.,* vol. 30, no. 8, pp. 4052–4057, Aug. 2015.

[3] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.,* vol. 30, no. 1, pp. 18–36, Jan. 2015.

[4] M. Zygmanowski, B. Grzesik, and R. Nalepa, "Capacitance and inductance selection of the modular multilevel converter," in *Proc. IEEE EPE,* Lille, France, Sep. 2013.

[5] J. Peralta, H. Saad, S. Dennetire, J. Mahseredjian, and S. Nguefeu, "Detailed and averaged models for a 401-level MMC-HVDC system," *IEEE Trans. Power Delivery,* vol. 27, no. 3, pp. 1501–1508, July 2012.

[6] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D. Xu, "Analysis of the phase-shifted carrier modulation for modular multilevel converters," *IEEE Trans. Power Electron.,* vol. 30, no. 1, pp. 297–310, Jan. 2015.

[7] W. Merwe, "Natural balancing of the 2-cell modular multilevel converter," *IEEE Trans. Ind. Appl.,* vol. 50, no. 6, pp. 4028–4035, Dec. 2014.

[8] J. Zhang and C. Zhao, "The research of SM topology with DC fault tolerance in MMC-HVDC," *IEEE Trans. Power Del.,* vol. 30, no. 3, pp. 1561–1568, June 2015.

[9] Y. Lee, S. Cui, S. Kim, and S. Sul, "Control of hybrid HVDC transmission system with LCC and FB-MMC," in *Proc. IEEE ECCE,* Pittsburgh, pp. 475–482, Sep. 2014.

[10] R. E. Torres-Olguin, A. Garces, M. Molinas, and T. Undeland, "Integration of offshore wind farm using a hybrid HVDC transmission composed by the PWM current source converter and line commutated converter," *IEEE Trans. Energy Conv.,* vol. 28, no. 1, pp. 125–134, Mar. 2013.

[11] J. Dai, D. Xu, and B. Wu, "A novel control scheme for current source converter based PMSG wind energy conversion systems," *IEEE Trans. Power Electron.,* vol. 24, no. 4, pp. 963–972, Apr. 2009.

[12] D. Shen and P. W. Lehn, "Modeling, analysis, and control of a current source inverter-based STATCOM," *IEEE Trans. Power Del.,* vol. 17, no. 1, pp. 248–253, Jan. 2002.

[13] Y. Ye, M. Kazerani, and V. H. Quintana, "Current source converter based STATCOM: modeling and control," *IEEE Trans. Power Del.,* vol. 20, no. 2, pp. 795–800, Apr. 2005.

[14] H. F. Bilgin et al., "Reactive power compensation of coal mining excavators by using a new generation STATCOM," *IEEE Trans. Ind. Appl.,* vol. 43, no. 1, pp. 97–110, Jan.-Feb. 2007.

[15] P. J. Grbovic, F. Gruson, N. Idir, and P. L. Moigne, "Turn-on performance of reverse blocking IGBT (RB IGBT) and optimization using advanced gate driver," *IEEE Trans. Power Electron.,* vol. 25, no. 4, pp. 970–980, Apr. 2010.

[16] H. Uemura, F. Krismer, and J. W. Kolar, "Comparative evaluation of T-type topologies comprising standard and reverse-blocking IGBTs," in *Proc. IEEE ECCE,* Denver, CO, pp. 1288–1295, Sep. 2013.

[17] P. Ladoux, N. Serbia, and E. Carroll, "On the potential of IGCTs in HVDC," *IEEE Journal of Emerging and Selected Topics in Power Electron.,* vol. PP, no. 99, pp. 1–1, May 2015.

[18] N. Binesh and B. Wu, "5-level parallel current source inverter for high power application with DC current balance control," in *Proc. IEEE IEMDC,* Niagara Falls, ON, pp. 504–509, May 2011.

[19] M. P. Aguirre, L. Calvino, and M. I. Valla, "Multilevel current-source inverter with FPGA control," *IEEE Trans. Ind. Electron.,* vol. 60, no. 1, pp. 3–10, Jan. 2013.

[20] Y. Zhang, T. Tang, L. Chen, F. Guo, and J. Li, "A novel voltage-source converter topology suitable for interface of renewable sources," in *Proc. IEEE ICEMS,* Tokyo, pp. 1–6, Nov. 2009.

[21] M. A. Perez, R. Lizana, C. Azocar, J. Rodriguez, and B. Wu, "Modular multilevel cascaded converter based on current source H-bridges cells," in *Proc. IEEE IECON,* Montreal, pp. 3443–3448, Oct. 2012.

[22] J. Liang, A. Nami, F. Dijkhuizen, P. Tenca, and J. Sastry, "Current source modular multilevel converter for HVDC and FACTS," in *Proc. IEEE EPE,* Lille, France, Sep. 2013.

[23] Y. Liu, Y. Tang, and J. Shi, "Application of small-sized SMES in an EV charging station with DC bus and PV system," *IEEE Trans. Appl. Supercond.,* vol. 25, no. 3, Jun. 2015.

[24] M. H. Ali, B. Wu, and R. A. Dougal, "An overview of SMES applications in power and energy systems," *IEEE Trans. Sust. Energy,* vol. 1, no. 1, pp. 38-47, Apr. 2010.

[25] Q. Song, W. Liu, X. Li, H. Rao, S. Xu, and L. Li, "A steady-state analysis method for a modular multilevel converter," *IEEE Trans. Power Electron.,* vol. 28, no. 8, pp. 3702–3713, Aug. 2013.

[26] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.,* vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[27] J. Pou, S. Ceballos, G. Konstantinou, V. G. Agelidis, R. Picas, and J. Zaragoza, "Circulating current injection methods based on instantaneous information for the modular multilevel converter," *IEEE Trans. Ind. Electron.,* vol. 62, no. 2, pp. 777–788, Feb. 2015.

[28] K. Ilves, S. Norrga, L. Harnefors, and H. P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Trans. Power Electron.,* vol. 29, no. 1, pp. 77–88, Jan. 2014.

[29] T. Christen and M. W. Carlen, "Theory of Ragone plots," *Journal of Power Sources, Elsevier,* vol. 91, pp. 210–216, Mar. 2000.

[30] M. M. C. Merlin and T. C. Green, "Cell capacitor sizing in multilevel converters: cases of the modular multilevel converter and alternate arm converter," *IET Power Electron.,* vol. 8, no. 2, pp. 350–360, Mar. 2015.

Mukesh M. Bhesaniya (S'15) received the B.E. degree in electrical engineering from the Sardar Patel University, Gujarat, India, in 2000 and the M.Tech. in electrical engineering from the Indian Institute of Technology Kanpur, India, in 2009, and is currently pursuing the Ph.D. degree in electrical engineering at the Indian Institute of Technology Bombay, Mumbai, India.

He is with the Department of Electrical Engineering, G. H. Patel College of Engineering and Technology, Gujarat. His research interests include power electronic converters, HVDC and flexible ac transmission systems.

Anshuman Shukla (S'04–M'08) received the M.Tech. and Ph.D. degrees in electrical engineering from the Indian Institute of Technology Kanpur, Kanpur, India, in 2003 and 2008, respectively. From 2008 to 2011, he was a Scientist with ABB Corporate Research Center, Vsters, Sweden. In 2008, he was a Research Associate in the Department of Electrical Engineering, University of South Carolina, Columbia, SC, USA. In 2011, he joined the Indian Institute of Technology Bombay, Mumbai, India, where he is currently an Assistant Professor in the Department of Electrical Engineering. His research interests include modulation and control of power-electronic converters, hybrid and solid-state circuit breakers, and applications of power electronics in power systems and electric drives.

Dr. Shukla is a recipient of the Young Engineer Award (2011) conferred by the Institution of Engineers, India.